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45. (New Claim) The image display device according to claim 44, wherein the active devices have been formed on a glass substrate by a process at a temperature of 600° C or lower.

REMARKS

This is in response to the Official Action currently outstanding in the above-identified application.

Claims 1-34 were originally presented. Claims 1-25 were elected for further prosecution in this application in the last filed Amendment in this application. Claims 26-34 have been cancelled, without prejudice. Claims 35 – 45 have been added. No claims have been amended or canceled herein. Accordingly, upon the entry of the foregoing Amendment, the claims under active prosecution in this application will be Claims 1 – 25 and 35 – 45.

A "**VERSION SHOWIN CHANGES MADE TO THE CLAIMS**" is attached as required by the Rules.

In the currently outstanding Official Action, the Examiner has:

- 1. Failed to acknowledged Applicants' claim of foreign priority under 35 USC 119(a)-(d), and to confirmed the safe receipt of the priority document for this application by the United States Patent and Trademark Office. Appropriate acknowledgement and confirmation of these matters in response to this communication is respectfully requested.**
- 2. Provided Applicants with a copy of a Notice of References Cited (PTO-892), and copies of the newly cited references.**

3. Provided Applicants with a copy of the Form PTO-1449 that accompanied their Information Disclosure Statement in the above-identified application duly signed, dated and initialed by the Examiner to confirm his consideration of the art cited therein
4. Indicated that Claims 1, 5, 10, 12, 14, 16, 18, 20, 22 and 24 are allowed. Applicants respectfully note that with respect to Claim 10, the Examiner's indication of allowance appears only at page 8 of the currently outstanding Official Action and **not** on the Summary page thereof.
5. Rejected Claims 8 and 9 under 35 USC 112, first paragraph, as containing subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected to make/use the invention. Specifically, the Examiner indicates a belief that there is no disclosure of the claimed initialization circuit in the disclosure. Claims 8 and 9, however, are indicated to be allowable if rewritten to overcome the rejections under 35 USC 112, first paragraph, and to include all of the limitations of their respective base claims and any intervening claims.
6. Objected to Claims 4 and 7 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form including all of the limitations of their respective base claims and any intervening claims.

7. Rejected Claim 2 under 35 USC 103(a) as being unpatentable over the Cairns, et al. reference (U.S. Patent No. 6,266,041).
8. Rejected Claims 3, 6, 11, 13, 15, 17, 19 and 21 under 35 USC 103(a) as being unpatentable over the Cairns, et al. reference in view of the Ogawa reference (U.S. Patent 6,018,331).
9. Rejected Claims 23 and 25 under 35 USC 103(a) as being unpatentable over the Cairns, et al. reference in view of the Ogawa reference, and the Ino, et al reference (U.S. Patent 5,903,014).
10. Provided Applicants with his a Statement of his Reasons for Allowance of the allowed claims specified hereinabove.

With regard to items 1 – 4 and 10, further detailed discussion in these Remarks is not believed to be necessary.

With regard to item 5, Applicants respectfully **traverse** the Examiner's rejection of Claims 8 and 9 under 35 USC 112, first paragraph, and request reconsideration.

In particular, Applicants respectfully call the Examiner's attention, for example, to page 15, lines 4-11; page 30, line 16 to page 31, line 6; page 32, line 15 to page 33, line 14; and to page 37, lines 10-18 of the present specification. Each of these sections of the specification, among others, indicates specifically that the shift register circuits contain (and/or may themselves in certain situations function as) initialization circuits. Indeed, the concept of initialization of the shift registers at power-on, and cyclically thereafter, is central to the concept of maintaining the shift registers in a collective state in which clock signal line loads and drive power do not need to be high.

Accordingly, Applicants respectfully submit that not only is the concept of initialization circuitry forming part of the shift register circuit disclosed in broad terms in the Summary of the Invention portion of the present specification, but also a detailed explanation of the fact that such circuitry is part of the shift register is clearly explained in the Detailed Description portion of the present specification in such a manner that a person of ordinary skill in the art would understand how to make and/or use the same.

In view of the foregoing, Applicants respectfully submit that the Examiner's rejection under 35 USC 112, first paragraph, is not supportable in view of the clear and extensive disclosures of the present specification. Reconsideration and a decision withdrawing the outstanding rejection under 35 USC 112, first paragraph, in response to this communication therefore is respectfully requested.

With respect to item 6, Applicants now have presented New Claims 35 – 45. The Examiner has indicated that Claim 4 would be allowable if presented in independent form including all of the limitations of its base claim and any intervening claims. New Claim 35 satisfies these criteria. Claims 36 – 45 present the subject matter of the remaining original claims that were directly or indirectly dependent upon original claim 2 in directly or indirectly dependent form from New Claim 35 and are submitted to be allowable for this reason. Note, the Examiner's objection to Claim 9 on the basis of insufficient specification disclosure has been dealt with, and in Applicants' estimation disposed of, hereinabove.

Allowance of New Claims 35 – 45 is response to this communication, therefore, is respectfully requested.

With respect to items 7 through 9 above, Applicants respectfully **traverse** the currently outstanding rejections under 35 USC 103(a) for the following reasons.

After detailed analysis of all of the potential possibilities attributable to the Examiner in support of his rejections under 35 USC 103(a) by implication or otherwise, Applicants have concluded that the Examiner's comments at page 3 of the currently outstanding Official Action must be directed erroneously to the limitations of originally filed Claim 3, rather than to the limitations of originally filed Claim 2.

In particular, after failing to be able to rationalize the Examiner's comments concerning his rejection of Claim 2 with the wording of Claim 2, Applicants realized that it is in Claim 3 that the concept of lowering the frequency of the clock signal during at least part of the period in which the pulse signal is transferred from the first to the last latch circuit is stated. Further, it was realized that it is to the latter concept that the Examiner's comments at page 3 of the currently outstanding Official Action are directed. Claim 2, on the other hand, is directed to initializing the shift register at regular intervals during its operation in substantially the same way that initialization at power on is accomplished in Claim 1.

Stated slightly differently, it appears that the Examiner's conclusion that: "It would have been obvious for one of ordinary skill in the art to provide the data line driver circuit comprising a first register which is split in small bank DDF's or latches and a further shift register operating at a lower frequency than the first register which is used to selectively applied a clock signal to each bank of DDF's or latches." is totally inapposite to originally filed Claim 2 of this application.

In view of the foregoing, and since the claims other than claim 2 that stand rejected under 35 USC 103(a) depend either directly or indirectly from original claim 2, Applicants respectfully submit that all of the Examiner's rejections under 35 USC 103(a) are defective and should be withdrawn. Reconsideration of the currently outstanding rejections under 35 USC 103(a) in response to this communication, therefore, is respectfully requested.

For each, and all, of the foregoing reasons, Applicants respectfully submit that the Examiner's currently outstanding rejections are in error, and that Claims 1 - 25 of this application are in condition for allowance. Consequently, reconsideration and allowance of this application in response to this communication are respectfully requested.

Applicants also believe that additional fees beyond those submitted herewith are not required in connection with the consideration of this response to the currently outstanding Official Action. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge and/or credit Deposit Account No. **04-1105**, as necessary, for the correct payment of all fees which may be due in connection with the filing and consideration of this communication.

Respectfully submitted,

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VERSION SHOWING CHANGES MADE TO THE CLAIMS

Deletions shown in brackets; Additions shown underlined.

Please add New Claims 35 – 45 as follows:

35. (New Claim) A shift register circuit, comprising:

- a plurality of latch circuits connected in series to sequentially transfer a pulse signal from one to another;
- a clock signal line transmitting a clock signal;
- a plurality of switching circuits performing electrical connection and disconnection between the clock signal line and the plurality of latch circuits, wherein at least one of the switching circuits electrically disconnects at least one of the plurality of latch circuits from the clock signal line at regular intervals;
- potentials at nodes of the plurality of latch circuits vary in accordance with the pulse transferred;
- the plurality of switching circuits each connect or disconnect corresponding latch circuits to or from the clock signal line in accordance with the potentials at the nodes of the corresponding latch circuits; and
- in at least part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has a frequency lower than in a normal operation period;
- wherein the frequency of the clock signal gradually increases in at least part of said period.

36. (New Claim) The shift register circuit according to Claim 35, wherein the frequency of the clock signal in said at least a part of the period is from 1/2 to 1/16 of a frequency of the clock signal in the normal operation period.
37. (New Claim) The shift register circuit according to Claim 35, wherein each latch circuit has an initialization circuit receiving an initialization signal from outside and initializing an internal node of the latch circuit in response to the initialization signal.
38. (New Claim) The shift register circuit according to Claim 35, wherein the clock signal has an amplitude smaller than an amplitude of a power-supply voltage of the shift register circuit.
39. (New Claim) The shift register circuit according to Claim 35, further comprising a buffer circuit supplying the plurality of latch circuits with a clock signal received from outside.
40. (New Claim) The shift register circuit according to Claim 35, wherein a clock signal received from outside has an amplitude different from an amplitude of the clock signal supplied to the plurality of latch circuits, and the shift register circuit further comprises a level shifter changing the amplitude of the clock signal received from outside.

41. (New Claim) An image display device of active matrix type, comprising:
 - a plurality of pixels arranged in a matrix form;
 - a data signal line supplying video data to be written to one of the plurality of pixels;
 - a scan line for controlling the writing of the video data to one of the plurality of pixels;
 - a data driver supplying the video signal to the data signal line in synchronization with a timing signal; and
 - a scan driver supplying a pulse signal to the scan line in synchronization with a timing signal;

at least one of the data driver and the scan driver comprising the shift register circuit according to claim 35.
42. (New Claim) The image display device according to claim 41, wherein the data driver has the shift register circuit, and initializes the potential level at each internal node of the plurality of latch circuits in the shift register circuit in synchronization with a vertical synchronous signal.
43. (New Claim) The image display device according to claim 41, wherein at least one of the data driver and the scan driver is formed on a substrate on which the plurality of pixels are also formed.
44. (New Claim) The image display device according to claim 43, wherein active devices included in at least the data driver comprise polysilicon thin-film transistors.

45. (New Claim) The image display device according to claim 44, wherein the active devices have been formed on a glass substrate by a process at a temperature of 600° C or lower.